CLAIMS

What is claimed is:

1. A method for superimposing a dithering signal onto a digital control signal having multiple pulses, the method comprising the steps of:

(a) nulling blocks of control signal pulses having at least one nulled pulse per block, such that each successive block of nulled pulses has at least the same number of nulled pulses as the block that immediately precedes the succeeding block; and

(b) nulling blocks of control signal pulses having at least one nulled pulse per block, such that each successive block of nulled pulses has an equal or less number of nulled pulses than the block that immediately precedes the succeeding block.

2. The method of Claim 1 further comprising the step of:

determining a period of the dithering signal;

wherein step (a) occurs over a first half of the dithering period and step (b) occurs over a second half of the dithering period.

3. The method of Claim 1 wherein the pulses are voltage pulses.

4. The method of Claim 1 wherein the nulled pulses have a voltage that is substantially equal to zero.

5. The method of Claim 1 wherein the control signal has a duty cycle that can be varied by modulating a pulse width.

6. The method of Claim 1 wherein each block of nulled pulses consists of consecutively nulled pulses with no intervening non-nulled pulses.

7. The method of Claim 1 wherein there is at least one pulse between succeeding blocks of nulled pulses.

8. The method of Claim 1 wherein the pulses are spaced at intervals that are substantially equal to the reciprocal of a frequency of the control signal.

9. A method for producing a dithered control signal by superimposing a dithering signal onto a digital control signal having multiple pulses, which comprises the steps of:

determining a time averaged duty cycle DC_{avg} of the dithered control signal;

determining an amplitude AMP of the dithered control signal;

determining a wave function WF that describes a wave shape of the dithered control signal; and

calculating a pulse duty cycle PDC for each pulse of the dithered control signal using the average duty cycle, amplitude, and wave function.

10. The method of Claim 9 wherein the wave function includes variables a time and a period as variables of the dithering signal.

11. The method of Claim 10 further comprising the steps of:

determining a frequency of the dithering signal; and

calculating the period of the dithering signal by taking the reciprocal of the dithering signal frequency.

12. The method of Claim 10 further comprising the step of varying the time.

13. The method of Claim 9 wherein the time is varied between zero and the period of the dithering signal.

14. The method of Claim 9 wherein the pulse duty cycle PDC is determined from the equation:

$PDC = DC_{avg} + AMP * WF$

15. The method of Claim 9 wherein the wave function is a sine wave.

16. The method of Claim 9 wherein the wave function is a cosine wave.

17. A method for dithering an output force generated by a transfer case actuator assembly, which steps comprise:

generating a digital control signal having multiple pulses;

modifying the digital control signal by nulling blocks of control signal pulses consisting of at least one nulled pulsed per block to produce a dithered control signal; and

varying the output force generated by the actuator assembly in response to the dithered control signal.

18. The method of Claim 17 further comprising the step of:

using the output force generated by the actuator assembly to move a clutch actuation mechanism.

19. The method of Claim 17 wherein each block of nulled pulses cause a corresponding dip in the output force generated by the actuator assembly.

20. The method of Claim 19 wherein the number of nulled pulses in a given block determines an amplitude of the corresponding dip in the output force generated by the actuator assembly.

21. The method of Claim 19 wherein the dip in output force generated by the actuator assembly causes a corresponding movement of a actuation mechanism.